REMARKS

In the last Office Action, the Examiner rejected claims 1, 2, 5, 6, 8, 9, 12, 13 and 16-23 under 35 U.S.C. §102(b) as being anticipated by Liu (US 5,768,617). Additional art was cited of interest.

In accordance with the present response, independent claims 1, 2, 5, 8 and 12 have been amended to incorporate the subject matter of dependent claims 18, 19, 6, 9 and 13, respectively, which have been canceled, and which are directed to the feature of temporarily stopping the generation of the readout completion notice signal by the signal generation means when the stored data amount measured by the data storage amount measurement means reaches a predetermined readout start storage amount. Independent claims 1, 2, 5, 8 and 12 have also been amended to recite with more specificity the feature of the output of the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data amount measured by the data storage amount measurement means. Independent claim 16 has been amended in a similar manner. Claims 21 and 23 have been canceled in light of the cancellation of claims 9 and 13, respectively. The foregoing amendments to the claims are supported by the descriptions in paragraphs [0063]-[0073] of the specification. Accordingly, no new matter has been entered.

Claims 1, 2, 5, 8, 12, 16, 20 and 22 are currently pending in this application.

Applicants most respectfully request entry of the foregoing amendment since it merely comprises revisions to independent claims 1, 2, 5, 8 and 12 to incorporate the subject matter of dependent claims 18, 19, 6, 9 and 13, respectively, which have been canceled and to recite with more specificity the feature of the output of the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data amount measured by the data storage amount measurement means, revisions to independent claim 16 similar to claims 1, 2 and 8, and cancellation of claims 21 and 23 in light of cancellation of claims 9 and 13, respectively. In addition, the amendment substantially narrows any appealable issues because it presents pending claims 1, 2, 5, 8, 12, 16, 20 and 22 in substantially narrowed form and cancels a substantial number of claims. Thus, no further consideration or search is necessitated by the amendment, and entry of the foregoing amendment does not impose a burden on the Examiner and should not be denied.

Applicants request reconsideration of their application in light of the foregoing amendments and the following discussion.

Brief Summary of the Invention

The present invention is directed to a memory interface device and corresponding memory interface method and to a modem device having the memory interface device.

Conventional memory interface devices and methods have been unable to reduce loads on a memory readout unit (e.g., a CPU of a PC card) during memory write and read procedures. As a result, data written by the memory write unit and read by a readout unit could not be processed with good efficiency, thereby degrading the processing speed of the memory interface device.

The present invention overcomes the drawbacks of the conventional art. Figs. 1-4 show an embodiment of a memory interface device 120 according to the present invention embodied in the claims. The memory interface device 120 controls memory access between a memory write unit 101 that writes data into a memory 100 and a memory readout unit 102 that reads the data from the memory 100. The memory write unit 101 is in compliance with a memory write procedure in which each time data is written into a memory 100 by a predetermined unit amount, it is confirmed that readout of the data from the memory 100 has been completed, and then the next memory write procedure of the data into the memory 100 is performed.

The memory interface device 120 includes a write detection section 10 that detects a memory write procedure in which the memory write unit 101 writes the predetermined unit

amount of the data into the memory 100. A signal generation section 107 generates, upon detection of the writing of the predetermined unit amount of the data by the write detection section 10, a readout completion notice signal that notifies the memory write unit 101, and thereby confirms, that the readout of the data from the memory 100 by the memory readout unit 102 has been completed so that the memory write unit 101 proceeds to perform a next memory write procedure of the data into the memory 100. A data storage amount measurement section 104 measures an amount of the data stored in the memory 100 during the memory write procedures. A memory readout control section 111 generates an interrupt signal with respect to the memory readout unit 102 to temporarily stop the generation of the readout completion notice signal by the signal generation section 107 when the stored data amount in the memory 100 reaches a predetermined readout start storage amount, and outputs the interrupt signal to the memory readout unit 102 so that the memory readout unit reads out all of the data stored in the memory 100 in accordance with the stored data amount measured by the data storage amount measurement section 104. A timer 108 counts a period in which writing of the predetermined unit amount of the data into the memory 100 by the memory write unit 101 is discontinued and outputs a timeout signal to the memory readout control section 111 when a value of the period count reaches a predetermined timer period. The memory readout control section 111 generates

and outputs the interrupt signal to the memory readout unit 102 even when the memory readout control section 111 receives the timeout signal output from the timer 108.

By the foregoing construction and corresponding functions, the present invention provides a memory interface device in which the number of interruptions during memory write and readout procedures is effectively reduced as compared to the conventional art. As a result, loads due to processing interruptions are reduced and data can be processed efficiently and integrally.

Applicants respectfully submit that amended claims pending claims 1, 2, 5, 8, 12, 16, 20 and 22 patentably distinguish from the prior art of record.

Traversal of Prior Art Rejection

Claims 1, 2, 5, 8, 12, 16, 20 and 22 were rejected under 35 U.S.C. §102(b) as being anticipated by Liu. Applicants respectfully traverse this rejection.

A rejection for anticipation under 35 U.S.C §102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In addition, the reference must be enabling and describe the applicants' claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention. In re Paulsen, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994); In re Spada, 15

USPQ2d 1655, 1657 (Fed. Cir. 1990). An anticipating reference must describe all of the elements and limitations of the claim in a single reference, and enable one of skill in the field of the invention to make and use the claimed invention. Merck & Co. v. Teva Pharm. USA Inc., 68 USPQ2d 1857, 1861 (Fed. Cir. 2003). Applying this law, Liu clearly does not anticipate claims 1, 2, 5, 8, 12, 16, 20 and 22.

Independent claim 1 requires a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the memory readout control means when a value of the period count reaches a predetermined timer period, the memory readout control means generating and outputting the interrupt signal to the memory readout unit even when the memory readout control means receives the timeout signal output from the timer.

The Examiner appears to be interpreting the timer 310 and corresponding functions described in col. 11, lines 39-67 of Liu as corresponding to the timer and corresponding functions recited in independent claim 1. With reference to Figs. 2-4 of Liu, if a host computer 210 reads data in a FIFO circuit 340 prior to the timer 310 counting down the first predetermined interval, processing transfers to done check 408, in which case a subsequent host interrupt timeout signal from the timer 310 is masked by a signal generated by an auto-read control circuit 350

in response to the host computer 210 starting to read data from FIFO circuit 340. If the host computer 210 fails to read the data in FIFO circuit 340 prior to completion of the first predetermined time interval, the timer 310 generates the host interrupt timeout signal. In response to the host interrupt timeout signal, the auto-read control circuit 350 returns processing to set a host interrupt 404 which issues another host computer interrupt. The assertion of the host computer interrupt by the auto-read control circuit 350 prevents the host computer 210 from timing out on a read sector command and requesting that the user abort, fail, or retry accessing that data in a disk drive 220.

However, Liu does not disclose or describe the timer and corresponding functions recited in independent claim 1. For example, Liu does not teach the specific relationship between the counting function of the timer and the writing of the predetermined amount of data into the memory by the memory write unit which requires such writing to be discontinued and a timeout signal outputted to the memory readout control means when a value of the period count reaches a predetermined timer period, and further that the memory readout control means generates and outputs the interrupt signal to the memory readout unit even when the memory readout control means receives the timeout signal output from the timer, as required by independent claim 1.

Should the Examiner maintain the rejection based on Liu, applicants respectfully request that the Examiner specifically point out how the specific description in col. 11, lines 39-67 anticipates the foregoing timer and corresponding functions recited in independent claim 1.

Moreover, amended independent claim 1 requires memory readout control means for generating an interrupt signal to temporarily stop the generation of the readout completion notice signal by the signal generation means when the stored data amount measured by the data storage amount measurement means reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data amount measured by the data storage amount measurement means. This feature, in combination with the feature of the timer and corresponding functions as set forth above, cover the sequences of operation of the memory interface shown in Figs. 3-4 and described in paragraphs [0063]-[0073] of the specification. No corresponding combination is disclosed or described by Liu.

Independent claims 2 and 8 have been amended in a manner similar to independent claim 1. No corresponding combinations are disclosed or described by Liu as set forth above for amended independent claim 1.

Amended independent claim 16 is directed to a modem device and requires memory readout control means for generating an interrupt signal to temporarily stop the generation of the readout completion notice signal when the stored data amount in the memory reaches a predetermined readout start storage amount, and for outputting the interrupt signal to the memory readout unit so that the memory readout unit reads out all of the data stored in the memory in accordance with the stored data mount measured by the data storage amount measurement means. Amended claim 16 further requires counting means for counting a period in which writing of the predetermined unit amount of the data into the memory is discontinued and for outputting a timeout signal to the memory readout control means when a predetermined value of the period count is reached, the memory readout control means generating and outputting the interrupt signal to the memory readout unit even when the memory readout control means receives the timeout signal. No corresponding combinations of features are disclosed or described by Liu as set forth above for amended independent claim 1.

Amended independent claim 5 is directed to a memory interface method and requires a step of generating an interrupt signal to temporarily stop the generation of the readout completion notice signal when the measured stored data amount reaches a predetermined readout start storage amount, a step of outputting the interrupt signal to the memory readout unit so

that the memory readout unit reads all of the data stored in the memory in accordance with the measured stored data amount, and a step of counting a period in which writing of the predetermined unit amount of the data is discontinued and a step of outputting a timeout signal when a value of the period count reaches a predetermined count period. Independent claim 12 has been amended in a similar manner. No corresponding combinations of steps are disclosed or described by Liu, as set forth above for the functions of the memory readout control means and timer recited in amended independent claim 1.

Therefore Liu cannot anticipate amended independent claims 1, 2, 5, 8, 12 and 16. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), citing Jamesbury Corp. v. Litton Industrial Products Inc., 225 USPQ 253, 256 (Fed. Cir. 1985) (The identical invention must be shown in as complete detail in the reference as contained in the claim.) Furthermore, Liu does not suggest the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Liu's system and method to arrive at the claimed invention.

Claims 20 and 22 depend on and contain all of the limitations of amended independent claims 8 and 12, respectively, and, therefore, distinguish from Liu at least in the same manner as set forth above for amended independent claims 8 and 12.

In view of the foregoing, applicants respectfully request that the rejection of claims 1, 2, 5, 8, 12, 16, 20 and 22 under 35 U.S.C. §102(b) as being anticipated by Liu be withdrawn.

In view of the foregoing, entry of this amendment and favorable reconsideration and passage of the application to issue are most respectfully requested. In the event the Examiner determines that something further need be done to place the application in allowable form, it is respectfully requested that the Examiner telephone the undersigned attorney at the below-listed number whereupon any outstanding matter will be promptly attended to.

Respectfully submitted,

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